The need to do more with less is a constant challenge for the semiconductor market. Manufacturers of semiconductor devices are constantly challenged to manage their costs including the cost of test. As shown in Figure 1, the ratio or percentage of ATE capital cost as a percentage of an IC’s average sales price (ASP) has progressively become smaller – moving from a high of 5% in 2001 to approximately 1% in 2010.

The cost of testing a device has not scaled at the same rate as the cost to produce these devices and subsequently, is now threatening to be a limiting factor in the price elasticity model associated with the electronics industry and the semiconductor industry specifically. Just keeping test costs even as a percentage of product cost requires test costs to be reduced in lock-step with overall product costs. Additionally, today’s semiconductor devices include a variety of digital, analog, and RF capabilities all combined in a single package or SoC (system on chip). The result is that test solutions must not only be cost effective but also flexible in order to address a range of circuit types including logic, memory, analog, MEMs and RF devices.

The challenge for today’s test engineers is to create new test methods and systems that can offer significantly lower test costs as well as address the need for configurable, flexible test solutions. COTS (commercial off the shelf) hardware has always played some part in semiconductor ATE solutions – sometimes augmenting “big iron” systems and in other cases, providing automated test setups for prototype device characterization. However, recent advancements in PXI digital test products now makes it possible for test engineers to address a range of ATE device test needs with the PXI platform. In particular, PXI digital products that offer tester per-pin features including a parametric measurement unit (PMU) per-pin architecture and per-pin programmability can now provide ATE semiconductor test capabilities at a fraction of the cost of traditional test systems.
**Semiconductor Test Needs**

Basic test needs for digital and mixed-signal devices include both DC parametric and functional tests. For the DC tests, all of a device’s pins must be characterized which requires a PMU. A PMU, which can source voltage / measure current or source current / measure voltage, must be able to access all of the device’s pins which require some type of switching / multiplexer if a single PMU is used. Once DC characterization is completed functional testing of the device can be performed. In this case, a digital instrument with sufficiently deep memory, per channel programmability (voltage, loads, and direction), and real-time compare provides the key features for performing functional tests. A basic setup that addresses these capabilities is shown in Figure 2.

![Figure 2 – System Configuration with PMU, Digital Instrument and Switching Matrix](image)

The combination of a PMU, switching network and digital instrument as shown in Figure 2 rapidly becomes unwieldy and performance limited for moderate to high pin count devices. Additionally, the combination of switching time and programming / measure time for a DC test can easily require 10’s or even 100’s of milliseconds, requiring long test times for the DC parametric tests. A better solution and one typically employed by proprietary ATE or “big iron” systems is to incorporate a PMU per pin or channel- resulting in superior test performance (both for speed and measurement accuracy). Today, there are PXI digital instruments (Figure 3) which offer both digital and per pin DC parametric test capabilities in a single slot, compact, 3U PXI format; offering test engineers lower cost test solutions, a simplified system architecture, and superior performance.

![Figure 3 – 3U PXI, 32 Channel Digital I/O with per pin PMU](image)
Performing DC Parametric Tests

As noted previously, a PMU can be used in one of two modes to perform dc characterization tests on the input and output lines of digital devices:

- Force voltage and measure current. With this method the PMU applies a constant voltage and using its on-board measurement capability it measures the current being drawn by the device/pin being tested. The voltage being supplied by the PMU can also be measured.
- Force current and measure voltage. With this method the parametric measurement unit either forces a constant current across a device or sinks a constant current from a device pin and then measures the resultant voltage. The PMU sink/source current also can be measured.

By combining a PMU per channel with digital test capabilities in one instrument, performing a range of DC tests on digital and mixed signal devices is significantly simplified. Common DC tests performed on digital devices include:

- VIH: (Voltage Input High), The minimum positive voltage applied to a device’s input which will be accepted by the device as a logic High
- VIL: (Voltage Input Low), The maximum positive voltage applied to a device’s input which will be accepted by the device as a logic Low
- VOL: (Voltage Output Low,) The maximum positive voltage from a device’s output defined to be the “guaranteed” maximum positive Low level for a specified load current
- VOH: (Voltage Output High) The minimum positive voltage from a device’s output defined to be the “guaranteed” minimum positive High level for a specified load current
- IIL: (Low Level Input Leakage) The input leakage current measured when the input is a logic Low
- IIH: (High Level Input Leakage) The input leakage current measured when the input is a logic High
- IOS(H): (High-level short-circuit output current) The short-circuit output current when the output is at a logic High
- IOS(L): (Low-level short-circuit output current) The short-circuit output current when the output is at a logic Low

Example: Performing VOH, VOL & IOS Tests

Output Voltage Level tests are used to verify the operation of a digital output when used under its specified loading conditions. They can also be used to simulate a worst-case loading condition to observe how a DUT will perform when an output is loaded beyond its specified limit, for example when shorted to ground. When performing these types of tests the test current range should be chosen to adequately test the output without damaging the device-under-test (DUT).

The following example shows how to perform a VOH test on a digital output. The purpose of this test is to ensure that the DUT can maintain an output voltage that is above its specified output high level while supplying its maximum rated drive current. For this test, the PMU is programmed to sink current from the DUT output, simulating a load condition.

Figure 4 shows how the DUT and Digital Instrument are connected.
To perform this test the DUT is powered up and one channel of the instrument (Ch1 in this example) is used to apply an input logic level that forces the DUT’s output to a logic High. Note that each instrument channel can be configured for PMU or digital I/O mode, providing the needed flexibility and functionality to support the VOH, VOL and IOS tests which require that a device’s outputs be programmed to the correct state prior to performing PMU measurements. A second digital channel (Ch2 in this example) is set to PMU Force Current/Measure Voltage mode with an initial current sink value that will not damage the DUT output pin. The PMU is then programmed to sink device current from minimum to maximum test values. At each test current value the DUT’s output voltage is measured to ensure it is within its specified voltage range for a logic High. The actual PMU test current can be measured also. These measured values can be used to generate an I-V Curve trace for possible fault-finding in the event of an output failure or simply for pass / fail testing. The testing technique described above can also be used for VOL and IOS testing. For the VOL test, the DUT’s output would be programmed to a logic Low and a specified load applied to the output with the output voltage level being measured to ensure it is within specification for the device. For the IOS parameter, the output would be programmed to the specified logic state, a short applied to the output, and resulting current measured.

Example: Performing Input Leakage Test (IIL, IIH)

Leakage current tests are performed by applying a constant voltage, in steps over a specified test voltage range, to the DUT input pin and measuring the input current at each step. As leakage currents are often in the uA range, the PMU should be set to its more sensitive current ranges to achieve more accurate measurements.

To perform an Input Leakage Test the DUT is powered up and the PMU pin is set to Force Voltage/ Measure Current Mode. At each input voltage setting the PMU measures the current being drawn by the input and then verifies the value against the DUT specification. The actual test voltage that the PMU is sourcing can be measured as well. The testing technique shown here can also be used for VIL and VIH testing.
Summary

With the availability of instrumentation that offers both digital and PMU per pin capabilities within a single slot, 3U PXI module, test engineers and system integrators now have the ability to develop semiconductor test system and applications that are comparable in features and performance to proprietary ATE systems. For example, to address the test needs for a 512 pin device, a PXI test system consisting of a 20 slot PXI chassis and (16) of the 32 channel digital instruments described above can be readily constructed with additional instrument slots available for other instrumentation or DUT (device under test) power – providing unmatched system functionality and density in a compact 3U PXI form factor. The high level of integration and channel density afforded by these digital instruments, coupled with the open architecture of PXI and wide selection of PXI products presents ATE test engineers with lower cost and more flexible test solutions for both present and future products – helping them to effectively address the “cost of test”.

Figure 5: Input Leakage test using the digital instrument’s PMU capability