Abstract: PXI High Speed Data Throughput Fundamentals
This paper gives a background of the PXI specification with a focus on its data protocols that form the foundation of its high data performance. Current product implementations of the standard and techniques to further take advantage of these capabilities are examined to provide insight into how these technologies might be exploited to expand the PXI market.

PXI is composed of multiple data protocols and form factors adopted from consumer products. By using robust and mature technologies, such as PCI, PCIe, cPCI, and cPCIe, the standard and its large compliment of products has helped mold the face of new T&M equipment. By utilizing these technologies, measurement devices can now be combined in complex topologies, taking advantage of the shared resources and customizable nature of PXI.

Upon the inclusion of PCIe into PXI, new capabilities have become available for instrument designers and system integrators. These new capabilities are just starting to be explored, with current products on the market beginning to show the advantages of this new standard. By recognizing current capabilities and limitations imposed, new architectures have become available to exploit the foresight of PCIe, while maintaining backward compatibility with existing PCI devices. By highlighting new possibilities in terms of performance and flexibility in the PXI domain, the future of this modular standard and its endless possibilities can begin to be explored.
PXI High Speed Data Fundamentals

PXI has emerged as a very flexible, capable standard for test and measurement equipment, shifting the modular instrument paradigm from stand-alone “box” instrumentation to a much smaller form factor to address markets with need for more granular components forming the modular ecosystem. A major difference between the PXI standard and common box instruments is the method for which data is moved through the system. This difference has been built on common off-the-shelf PC communication protocols and provides many benefits, namely improved data throughput over traditional message based systems which exhibit higher latency and protocol overheads. To understand the benefits of the data movement capabilities of PXI, the foundational protocols need to be understood. With this understanding, there new data movement techniques can be applied to new product offerings and provide a look at what new technologies can provide to the standard for which to expand the market capabilities of PXI.

The original PXI was based on the 32-bit PCI standard, a parallel peripheral interconnect technology that typically provides 133 MB/s of shared bandwidth amongst the peripherals connected. Each parallel bus can support multiple devices but practical electrical loading limitations require bridges to expand these busses for high peripheral count environments. As a peripheral interconnect standard, the modular devices are controlled via software in a register based manner from a host controller. The PCI specification also provides many enhanced features, such as peer-to-peer communication between peripherals’ memory spaces enhancing the data bandwidth capabilities by facilitating parallelism and host independence through the implementation of multiple bus masters. The main application of peer-to-peer communication was direct memory access (DMA) that provided processor independence during transfer of data between peripherals and host memory by allowing peripherals to master the PCI bus. As higher performance devices eventually became limited by the protocol’s performance, new versions of the PCI standard emerged in the form of wider parallel busses and higher frequency clocking, such as PCI-X, affected the original electrical loading limitations, restricting these higher performance PCI variants to very small peripheral counts. Another unfortunate side affect of PCI is its poor error handling capabilities which most people are familiar with through the dreaded Blue Screen of Death (BSoD) which commonly results from a corrupt PCI communication. It wasn’t until the advent of PCI Express that extremely high performance, robust, modular peripherals became available.

PCI Express builds on PCI’s software and interface structure from PCI, allowing complete backward compatibility with PCI host systems and their software. PCIe’s main differentiation is exhibited in its physical implementation. Moving beyond the limitations of the parallel bus structure, PCIe employs a point-to-point based communication scheme, utilizing the benefits of differential signaling technology for extremely high speed serial data transmission as well as moving away from the bridge scheme in PCI to a switching scheme isolating each peripheral. Across the differential lines, data is communicated via packets with integrity evaluation at many levels, most importantly the physical layer can recognize signal integrity errors and request new
packets transparent to the host (fewer BSoDs!). Another benefit of point-to-point connections is the removal of a parallel bus; PCIe’s serial communication implies each peripheral has dedicated bandwidth to its upstream host which can be increased by adding multiple lanes per link. These dedicated links support the following signaling speeds (and their theoretical data rates removing encoding overhead): Gen1 at 2.5 Gb/s (250 MB/s/lane), Gen2 at 5 Gb/s (500 MB/s/lane) and Gen3 at 8 Gb/s (1 GB/s/lane). Since each link connected through a switch topology has dedicated bandwidth to its upstream switch port, the peer-to-peer technology originally employed in PCI gets a major boost in parallelism. With PCIe switches that allow multiple, simultaneous peer-to-peer communications, systems with an efficient switching topology can create massive parallelism in data bandwidth. Since latencies are dependent on the depth of the switch topology, it is apparent that the design of the system’s PCIe topology is an important consideration in reducing point-to-point data transmission times. All of these advantages, from massively increased data throughput to parallel data movement capabilities, are beginning to benefit the test and measurement space with their adoption of PXI Express.

As the PXI industry adopted the PCIe standard (through Compact PCI Express, the ruggedized form of PCIe), vendors had to make tradeoffs to be compatible with the large number of legacy products while moving into the higher speed domain. Since the hybrid compatible slot in PXIe is capable of providing 32-bit PCI and PCIe protocols it is the logical choice for every slot of a chassis, but due to the complexities of routing so many signals as well as the board space required of the ICs and connectors, vendors have created PXIe systems with a mix of PCI, hybrid, and first generation PCIe-only slots. These chassis have also strictly implemented the 4-Link configuration in which 4 links are supported from the system controller, all of which are of maximum width of 4 lanes. Each of the system links has traditionally been connected to a separate switch, segregating direct peer-to-peer connectivity resulting in switch topologies that require traffic to traverse additional switches for some point-to-point communications as well as creating a 4 lane wide bottlenecks to the host, reducing the usable slot capabilities of 8 lanes. This concept is shown in Figure 1.
Figure 1: A common 18-slot PXIe chassis layout. Each switch creates a 4 lane bottleneck, not allowing utilization of the maximum 8 lanes allowed by the specification. This topology also requires peer-to-peer data from different switches to be connected through an external switch.

On systems with a maximum of 4 lanes running at Gen1 PCIe speeds, a maximum theoretical bandwidth limited to 1 GB/s per slot can be expected. Furthermore, with 4 links connecting to the host controller, we can expect applications to be able to only take advantage of 4 GB/s of controller bandwidth.

The main applications that have taken advantage of the PCIe capabilities of these new chassis are those requiring high data bandwidths, including high-speed digitizers, arbitrary waveform generators, DAQs, oscilloscopes, FPGA co-processors, and mass storage devices. Recently, peer-to-peer communication has been enabled in a number of devices by having software control over their DMA destinations; for example, a program may allow a capable digitizer to directly transfer data to FPGA co-processors to perform real-time calculations without the intervention of the host processor, freeing up the processor to do other tasks. In systems that divide its slots into segments by connecting them to multiple switches, peer-to-peer communication is often limited to these boundaries (commonly 4 slots wide) unless another switch is present in the host controller, further increasing latency of communications.

The current available PXI infrastructures are limited by the restrictions imposed by their switch topologies, increasing latency and reducing lane counts, while designing in slot limitations through their dedicated, non-hybrid support of either legacy or express capabilities. Through understanding the current technologies and market offerings, Agilent Technologies’ new
M9018A 18-slot PXIe chassis has taken greater advantage of the extended capabilities of PXIe by creating an open infrastructure through its transparent switch topology, second generation (Gen2) implementation of PCIe, full legacy and express compatibility in every peripheral slot, and utilizing 2- or 4-Link host controller configurations to allow utilization of the 8 lane slots. The all hybrid slot configuration is shown in Figure 2.

![Figure 2: Agilent Technologies’ New M9018A 18-Slot PXIe Chassis](image)

All of this allows peripherals to have up to 4 GB/s available bandwidth and controllers to have up to 8 GB/s system bandwidth. With a unique switch topology, the entire system can be configured to be a single peer-to-peer segment, allowing all slots to communicate with each other directly without the need for host intervention, as shown in Figure 3 (for devices that are capable of this of course).
Figure 3: Example of the M9018A reconfigurable switch fabric. In this example configuration, peer-to-peer communication can take place from any slot to any other slot without data leaving the chassis’ switches, reducing data latency and removing the requirement to having another PCIe switch in the system slot.

By creating such a fast and open infrastructure, massive bandwidth systems have become available and give peripheral creators the opportunity to create the next generation of high-speed integrated test and measurement systems.

Whether it is implementing next generation PCI Express or taking advantages of techniques such as peer-to-peer communication with low latency, open switch topologies, engineers will be looking to PXISA and its participating companies to continue to push the technology for PXIe products to the next level.